EXHIBIT 8

[redacted]

US005694466A

United States Patent [19]

Xie et al.

[11] Patent Number: 5,694,466

[45] Date of Patent: Dec. 2, 1997

[54] **DTMF DETECTOR SYSTEM AND METHOD WHICH PERFORMS IMPROVED TWIST COMPUTATION AND THRESHOLDING**

[75] Inventors: **Zheng-yi Xie**, Richardson; **John G. Bartkowiak**, Austin, both of Tex.

[73] Assignee: **Advanced Micro Devices, Inc.**, Sunnyvale, Calif.

[21] Appl. No.: **588,407**

[22] Filed: **Jan. 18, 1996**

Related U.S. Application Data

[63] Continuation of Ser. No. 563,973, Nov. 29, 1995, Pat. No. 5,644,634, and a continuation of Ser. No. 585,530, Jan. 11, 1996, Pat. No. 5,588,053.

[51] **Int. Cl.**[6] **H04M 1/50**

[52] **U.S. Cl.** **379/386**; 379/282; 379/283

[58] **Field of Search** 379/386, 351, 379/282, 283, 6, 77

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,853,958	8/1989	Rapibour et al.	379/386
5,257,309	10/1993	Brandman et al.	379/283
5,319,703	6/1994	Drory	379/351
5,325,427	6/1994	Dighe	379/386
5,353,345	10/1994	Galand	379/386
5,408,529	4/1995	Greaves	379/386
5,426,696	6/1995	Zimbrek	379/386
5,428,680	6/1995	Murata et al.	379/386
5,495,526	2/1996	Cesaro et al.	379/386

OTHER PUBLICATIONS

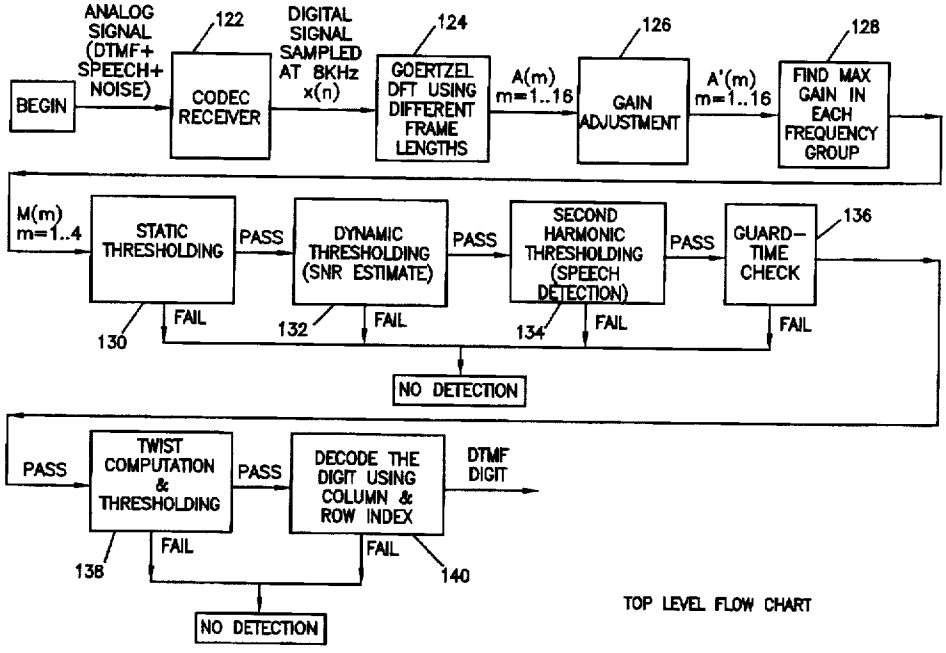
Digital Signal Processing Applications Using the ADSP-2100 Family, vol. 1, by The Applications Engineering Staff of Analog Devices, DSP Division, Edited by Amy Mar, 1992 by Analog Devices, Inc., pp. 441–500.

Primary Examiner—Krista M. Zele
Assistant Examiner—Jacques M. Saint-Surin
Attorney, Agent, or Firm—Conley, Rose & Tayon; Jeffrey C. Hood

[57] **ABSTRACT**

An improved dual tone multifrequency (DTMF) or multi-tone signal detector which more efficiently and reliably detects DTMF signals. The present invention performs twist computations only when the signal has become stable, thus achieving more accuracy and reliability. The DTMF detector receives a plurality of digital samples of a received signal and calculates energy values for each of the plurality of different uncorrelated frequencies. The DSP then determines maximum values of the energy values for each of the two or more frequency groups, referred to as M(1) and M(2), to detect the plurality of tones in the received signal. The DTMF detector then performs improved twist computation and thresholding. The DTMF detector first determines if the M(1) and M(2) values of the respective frame being examined have the same indices. If so, the DTMF detector compares each of the M(1) and M(2) values of the respective frame being examined with the M(1) and M(2) values of the immediately prior frame, referred to as M'(1) and M'(2), and determines if the M(1) and M(2) values of the current frame are greater than the M'(1) and M'(2) values of the prior frame. If the M(1) and M(2) values of the current frame are greater than the M'(1) and M'(2) values of the prior frame, then the DTMF detector calculates a twist value using the maximum energy values M(1) and M(2) for the current frame being examined.

29 Claims, 11 Drawing Sheets



TOP LEVEL FLOW CHART

Contact

www.linkedin.com/in/robjork
(LinkedIn)

Top Skills

Go-to-market Strategy
Channel
Mobile

Publications

System Level Failure Analysis Process: Making FA a Value Add Proposition

Roger Bjork

President and Owner at Pilgrimage With Purpose
Round Rock

Summary

Executive leader with cross-functional and global experience. Excellent leader of people, with a reputation for building great organizations and building bridges between peer organizations. Experience includes executive leadership in R&D (hardware and software), Strategy & Business Development, and Marketing. Now focused on delivering niche hospitality and travel services businesses.

Experience

Pilgrimage With Purpose
President and Owner
September 2018 - Present (3 years 6 months)
78681 Round Rock, Texas

Building unique opportunities for modern day pilgrims to intensify their relationship with God through engaging spiritual encounters and deepening their biblical context and knowledge at holy sites around the world. Come explore your Catholic heritage. www.PilgrimageWithPurpose.com

Self
Retired global executive
April 2017 - Present (4 years 11 months)
Austin-based

In addition to travel, golf, and woodworking, am currently engaged in helping expand the footprint of a major central Texas charity and service organization, as well as serving on my parish Finance Council. Also developing business model and plan for new startup ventures.

Dell
17 years 7 months

Global Marketing Director, Data Security Solutions and Thought Leadership Programs
December 2014 - April 2017 (2 years 5 months)
Austin, TX

Dual role responsible for the global product launch of Dell's portfolio of data security solutions enabling secure cloud-based file sync and share collaboration. Also responsible for development and execution of Dell's Thought Leadership marketing programs to propel the entire data security solutions portfolio to the forefront of customer consideration. Both roles leverage multi-discipline and cross-functional influence and execution, executive leadership, and the utmost energy.

Director, Enterprise Mobility Solutions Go-To-Market and Business Development

February 2010 - December 2014 (4 years 11 months)

Marketing planning, Channel Support, Channel Development, Business Development. All centered around Enterprise Mobility Solutions to help our enterprise customers embrace the explosion of mobile devices. Driving solutions to build an Enterprise Mobile Strategy, Manage Devices and Applications, and Secure mobile connections.

Consumer System Engineering/Architect and Strategy Development

June 2008 - January 2010 (1 year 8 months)

Responsible for automation technologies enabling self-diagnosis and self-healing of Dell consumer PCs. Resulted in increased customer satisfaction and $$ millions in annual customer support savings.

Senior Manager, WW Services Architecture and Advanced Planning

January 2005 - May 2008 (3 years 5 months)

Chief Architect and Portfolio Planning for Dell's innovative support automation portfolio. Enables product self-healing, a superior experience in custome self-help, and enhanced assisted support from Dell's global support team.

Senior Manager - Global Sustaining Engineering & Failure Analysis

October 1999 - December 2004 (5 years 3 months)

Managed a global engineering team responsible for implementing quality improvements, cost reductions, and feature enhancements to existing and shipping PC desktop/laptop portfolio. Developed robust Failure Analysis processes between Dell and its suppliers to rapidly identify root cause failures, resulting in $$ millions in savings due to rapid introduction of correction actions.

Siemens

17 years

Director of Engineering

1997 - 1999 (2 years)

Executive leadership for US R&D operations (hardware, software, mechanical, & quality engineering) for consumer cordless telephones. Responsible for on-time, on-budget, on quality introduction of new consumer telephony products.

Engineering Management

1982 - 1997 (15 years)

Responsible for global software development for new consumer telephony products.

Education

Texas A&M University

BS CS, Computer Science · (1978 - 1982)

US006829307B1

(12) **United States Patent**
Hoo et al.

(10) **Patent No.: US 6,829,307 B1**
(45) **Date of Patent: Dec. 7, 2004**

(54) **EXPRESS BIT SWAPPING IN A MULTICARRIER TRANSMISSION SYSTEM**

(75) Inventors: **Louise Min Chuin Hoo**, Stanford, CA (US); **Atul Arvind Salvekar**, Stanford, CA (US); **Carlos Aldana**, Stanford, CA (US); **John M. Cioffi**, Los Altos Hills, CA (US); **Peter Chow**, Los Altos, CA (US); **James Carlo**, Dallas, TX (US)

(73) Assignees: **The Board of Trustees of Leland Stanford Junior University**, Palo Alto, CA (US); **Texas Instruments, Inc.**, Dallas, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/513,716**

(22) Filed: **Feb. 24, 2000**

Related U.S. Application Data

(60) Provisional application No. 60/123,096, filed on Mar. 5, 1999, provisional application No. 60/122,121, filed on Mar. 2, 1999, and provisional application No. 60/121,359, filed on Feb. 24, 1999.

(51) **Int. Cl.**[7] **H04K 1/10**

(52) **U.S. Cl.** **375/260**; 375/295; 375/222; 375/358

(58) **Field of Search** 375/260, 316, 375/222, 214, 358, 295

(56) **References Cited**

U.S. PATENT DOCUMENTS

5,400,322 A 3/1995 Hunt et al.

(List continued on next page.)

OTHER PUBLICATIONS

John M. Cioffi, "The Essential Merit of Bit–Swapping". ANSI Contribution T1E1.4/98–318R1, Dec. 1998.*

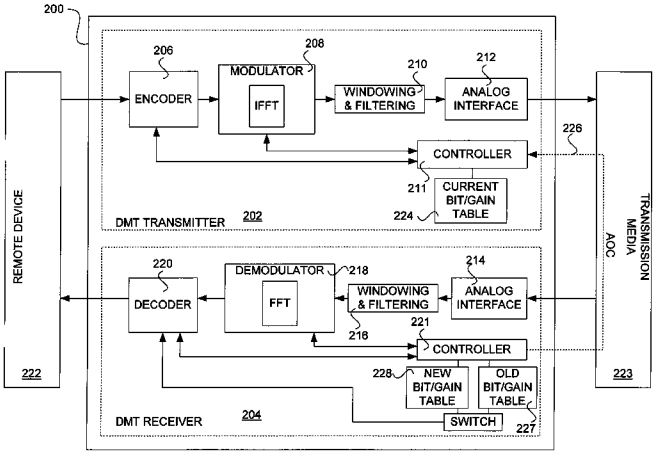
(List continued on next page.)

Primary Examiner—Temesghen Ghebretinsae
(74) *Attorney, Agent, or Firm*—Beyer Weaver & Thomas, LLP

(57) **ABSTRACT**

Methods and devices for adaptively changing a parameter (such as sub-carrier bit allocation and/or gain) in a multi-carrier communication signal are described. In a method aspect, a unit that determines a need for a change sends an express change request to a second unit. The change request identifies one or more specific sub-carrier carrier to be altered and a desired value for the parameter to be changed for each identified sub-carrier. The requesting unit then monitors the communication signal it receives to determine whether the requested change has been implemented. The determination of whether the requested change has been implemented is based at least in part upon an analysis of a portion of the received communication signal that was intended to be changed. In another aspect of the invention, the change request command includes a header, a control field, at least one sub-carrier identifier, at least one desired parameter value indicator, and an error field. The header identifies the command as a change request command. The control field includes a tone count that indicates the number of tones to be altered. Each sub-carrier identifier identifies a specific sub-carrier to be altered and each desired parameter value indicator identifies a desired parameter value for its associated sub-carrier. The error field permits the unit receiving the change request to detect whether there is an error in its interpretation of the change request command.

30 Claims, 6 Drawing Sheets



Contact

www.linkedin.com/in/kim-chang-61210b7 (LinkedIn)

Top Skills

Telecommunications
Wireless
LTE

Languages

Chinese

Kim Chang

Senior Director at Huawei
Plano

Summary

Wireless Advanced Research & Standards

Experience

Huawei
17 years

Senior Director
August 2009 - Present (12 years 7 months)

NA Corporate Standards

Senior Director
2005 - August 2009 (4 years)

Wireless Advanced Research & Standards

TAMC VC
Sr. Investment Manager
2000 - 2005 (5 years)

Nortel Networks
Manager, CDMA Standards
1994 - 2000 (6 years)

Education

The University of Texas at Austin
BSEE, Solid State · (1989 - 1993)

Texas A&M University
MSEE, Digital Comm, Analog Circuit Design · (1993 - 1995)

US006549512B2

(12) **United States Patent**
Wu et al.

(10) **Patent No.: US 6,549,512 B2**
(45) **Date of Patent: *Apr. 15, 2003**

(54) **MDSL DMT ARCHITECTURE**

(75) Inventors: **Song Wu**, Plano, TX (US); **Donald P. Shaver**, Dallas, TX (US); **Yaqi Cheng**, Rowlett, TX (US)

(73) Assignee: **Texas Instruments Incorporated**, Dallas, TX (US)

(*) Notice: This patent issued on a continued prosecution application filed under 37 CFR 1.53(d), and is subject to the twenty year patent term provisions of 35 U.S.C. 154(a)(2).

Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/105,134**

(22) Filed: **Jun. 25, 1998**

(65) **Prior Publication Data**

US 2002/0172146 A1 Nov. 21, 2002

Related U.S. Application Data

(60) Provisional application No. 60/050,707, filed on Jun. 25, 1997, and provisional application No. 60/050,753, filed on Jun. 25, 1997.

(51) **Int. Cl.**[7] **H04J 11/00**
(52) **U.S. Cl.** **370/210**; 375/233; 375/350
(58) **Field of Search** 370/276, 419, 370/445, 463, 465, 210, 498, 507, 545, 468, 487, 295, 206, 480, 484, 477; 375/260, 221, 222, 225, 229, 345, 371, 231, 233, 350; 708/323; 455/245.1

(56) **References Cited**

U.S. PATENT DOCUMENTS

4,683,578	A	*	7/1987	Betts et al.	375/98
5,400,322	A	*	3/1995	Hunt et al.	370/19
5,479,447	A	*	12/1995	Chow et al.	375/260
5,999,563	A	*	12/1999	Polley et al.	375/222
6,052,380	A	*	4/2000	Bell	370/445
6,389,062	B1	*	5/2002	Wu	375/222

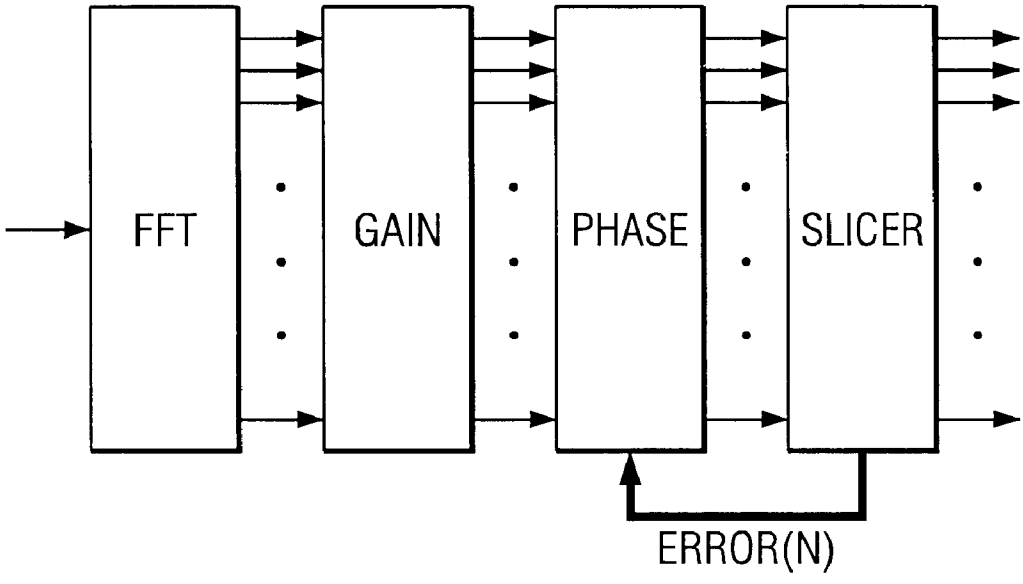
* cited by examiner

Primary Examiner—Alpus H. Hsu
Assistant Examiner—Duc Ho
(74) *Attorney, Agent, or Firm*—Warren L. Franz; Wade James Brady, III; Frederick J. Telecky Jr.

(57) **ABSTRACT**

A DMT device having an analog front end for receiving an analog signal, a converter for converting the analog signal to a digital signal, a FFT for converting the digital signal from the time domain to the frequency domain and feeding the digital signal to a frequency domain equalizer having variable coefficients for flattening the converted digital signal. The frequency domain equalizer includes a gain corrector coupled to the FFT to compensate the channel frequency rolloff and make each tone approximately the same amplitude before phase rotation and a phase rotator portion responsive to the output of the gain corrector to track small channel variation. Also included is circuitry for updating the coefficients of the frequency domain equalizer, preferably in the form of a slicer for controlling the frequency domain equalizer by feeding back an error signal thereto. The error signal is preferably fed back to the phase rotator portion of the frequency domain equalizer.

6 Claims, 5 Drawing Sheets



US005128619A

United States Patent [19]

Bjork et al.

[11] Patent Number: 5,128,619

[45] Date of Patent: Jul. 7, 1992

[54] SYSTEM AND METHOD OF DETERMINING CABLE CHARACTERISTICS

[76] Inventors: Roger A. Bjork, 2904 Oak Bend, Round Rock, Tex. 78681; John T. Chapman, 1035 Aster Ave. #2143, Sunnyvale, Calif. 94086; Harry L. Cochrane, Rte. 2 Box 423, Liberty Hill, Tex. 78642; Timothy L. Wilson, 9200 N Plaza #2510, Austin, Tex. 78753

[21] Appl. No.: 759,044

[22] Filed: Sep. 5, 1991

Related U.S. Application Data

[63] Continuation of Ser. No. 332,862, Apr. 3, 1989, abandoned.

[51] Int. Cl.[5] G01R 31/11

[52] U.S. Cl. 324/533; 324/534; 379/26; 379/6

[58] Field of Search 324/533, 532, 534; 379/6, 24, 26, 30, 32

[56] References Cited

U.S. PATENT DOCUMENTS

2,800,627	7/1957	Oudin et al.	324/533
3,683,282	8/1972	D'Amato et al.	324/614
4,165,482	8/1979	Gale	324/523
4,325,022	4/1982	Pelletier	324/533
4,739,276	4/1988	Graube	324/534
4,766,386	8/1988	Oliver et al.	324/533
4,766,549	8/1988	Schweitzer, III et al.	324/533
4,768,203	8/1988	Ingle	379/6

FOREIGN PATENT DOCUMENTS

2073549	10/1981	United Kingdom	379/24

OTHER PUBLICATIONS

"Communications Network Testing", G. Immeyer et al, *IBM Technical Disclosure Bulletin*, vol. 22, No. 8A, Jan. 1980, pp. 3334–3335.

"Time Domain Reflectrometry: Versatile New Way of Testing Cable", J. Trudel, *Telephony*, Jan. 19, 1976.

"TDR for Cable Testing", TEK 1500 Series Metallic Cable TDR's, Application Note AX-3241-1.

"Measurement System for Attenuation, Numerical Aperture, Dispersion, and Optical Time Domain Reflectometry in Infrared Optial Fibers", *Proc SPIE Int. Soc. Opt. Eng.*, vol. 618, 1986, pp. 151–158.

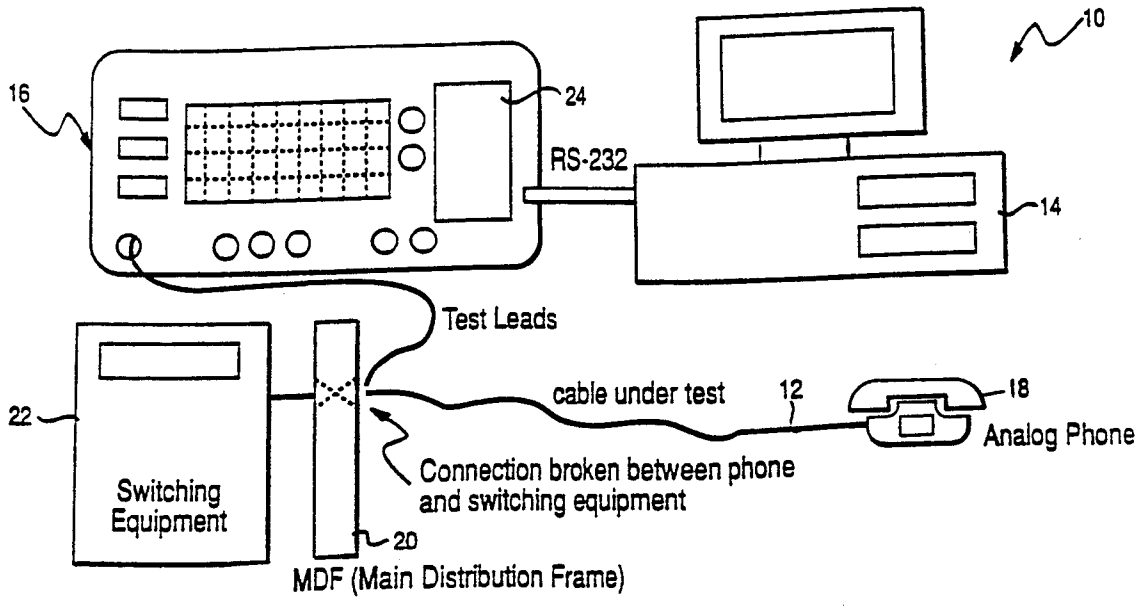
"Measuring System for ISDN", *Journal Electron, Eng.*, Dec. 1987, pp. 56–57.

Primary Examiner—Kenneth A. Wieder
Assistant Examiner—Maura K. Regan
Attorney, Agent, or Firm—Perman & Green

[57] ABSTRACT

A method of and system for automatically determining length, attenuation, impedance and existence of bridge taps on installed communication cable having access to only one end of the cable. A waveform, which includes incident and reflected pulses, is analyzed to determine the presence of significant pulses. The presence of only one positive significant pulse indicates the absence of any discontinuities and facilitates the calculation of a signal-to-noise ratio which determines whether the cable will support the operation of digital communication thereon. The presence of more than one positive significant pulse or a negative pulse indicates the presence of at least one fault on the cable which prevents the operation of digital communication on the cable.

14 Claims, 4 Drawing Sheets



Contact

www.linkedin.com/in/terrycole (LinkedIn)
home.earthlink.net/~terry.cole (Personal)
streetyouth.blogspot.com (Blog)
motsdots.etsy.com (Other)

Top Skills

Public Speaking
Semiconductors
Program Management

Certifications

Spring '16 Release

Patents

Software modem with hidden authentication commands
Method and apparatus for using low power training
Method and apparatus for preventing radio communication system access by an unauthorized modem
Connection manager with remote portal service

Terry L Cole

Missionary, Founder and Executive Director, Street Youth Ministry
Austin

Summary

System analyst and solution architect in the fields of mission work, homeless services, youth and young adult development, and application of Salesforce.org to small but nightly nonprofits. Former computer and electrical engineer including technology collaborator for xDSL and WiFi standardization and proliferation.

It is my goal to actively pursue my calling to deliver ministry to the young homeless and addicted in Austin, through direct community based services, community education, and advocacy. I also desire to see all nonprofits reach their full potential by use of best practices and to see my Austin community whole and fully interlinked.

Strong Day Statement: I am strong when I make progress toward future changing goals with a group of people who are willing to teach and share their passions.

Specialties: Salesforce.org, NPSP, Application of strengths-based solution-focussed to youth and young adult homelessness, Public Speaking, Governance (public, technical, and non-profit) , Software architecture and design, Program management, Small but mighty non-profit management.

Experience

Street Youth Ministry
Missionary and Founding Executive Director
August 2008 - Present (13 years 7 months)
Austin, Texas Area

Missionary and founder of Street Youth Ministry. Mission: To know, love, and serve street-dependent youth. We serve 80 to 100 street-dependent young people every week, providing them faith-based service, access to save spaces, food, clothing, and strength-based solution-focussed help. We work with hundreds of volutneers. We work with many church partners to improve

resources available in our city for street youth. We provide public speaking to groups of 20 or more. We provide fee-based consulting to any agency challenged by their relationship to the homeless community.

Salesforce.org
Board Member for Nonprofit Success Pack
September 2016 - Present (5 years 6 months)

Covenant Presbyterian Church
24 years

Member
1998 - Present (24 years)

Active member of Covenant Presbyterian Church (www.covenant.org).

Mission Committee Chair
May 2008 - May 2012 (4 years 1 month)

Oversee budget, development, volunteerism and all relationship development for local and global mission.

Music Committee Chair
August 2000 - April 2004 (3 years 9 months)

Committee chair of the music sub-committee of the worship committee of Covenant Presbyterian Church (www.covenant.org).

LifeWorks Austin
8 years 7 months

Adjunct Staff Member for Street Outreach
July 2008 - December 2016 (8 years 6 months)
Austin, Texas Area

Serves as street outreach drop-in center worker, brief therapy counselor, and group leader.

Intern, Youth Street Outreach
June 2008 - June 2008 (1 month)

I am interning at Lifeworks, Austin in their Youth Street Outreach division, under supervision of the director, LMSW, and the counselor for group services, MSW. I am learning and applying harm reduction theory, theory of personal change, and delivering basic services to youth service partners up to the age of 24. I make referrals to about a hundred different social service agencies in Austin. I have about 100 contacts with homeless youth per week.

IEEE 802.11
Working Group Technical Editor
2002 - March 2010 (8 years)

Responsible for publication of each IEEE 802.11 document. Responsible for combining each published amendment into a single master document. Task Group 802.11ma Editor. Technical editing for this revision of 802.11. Member Major contributions and participation to complete 802.11g Amendment.

Help for All Nations (www.creamandsugar.org)
Intern, homeless ministry
June 2008 - May 2009 (1 year)

I am an intern with Help for the Nations, a non-denominational non-profit religious ministry for the homeless, particularly young travelers, in Austin, Texas. I work under the supervision of three missionaries from Switzerland and Germany (who have been serving in Austin for 5 years) and who are sent by Walter Heidenreich's organization in Germany, Help International (http://www.helpinternational.de/e/index.html) and Free Christian Youth Fellowship (http://www.fcjg.de). I serve coffee, cool water, oatmeal, and noodle soup in a portable trailer to homeless people from central business district near the University of Texas. The homeless receive love just as they are and are able to ask questions, ask for guidance, and seek assistance in dealing with homelessness, loneliness, difficulties, and addiction.

AMD
13 years 5 months

AMD Fellow
January 2008 - August 2008 (8 months)

CTO for Client I/O Technologies

AMD Fellow
August 2006 - December 2007 (1 year 5 months)

Wireless strategy for the Office of Strategy Management

AMD Fellow
August 2005 - August 2006 (1 year 1 month)

Technical adviser to the general manager of the embedded division of AMD. Program manager of a new consumer electronic embedded processor Au1200 and software for the personal media player application.

Fellow
2000 - August 2005 (5 years)

Advanced Development Labs & Personal Connectivity Solutions Group. Analysis of emerging communication opportunities in PC and low power handheld market with an emphasis on wireless. Advanced hardware and software architectures for EDGE WWAN, WLAN 802.11 and other wireless products. Defined architecture of WWAN EDGE solution, including DSP instruction set. Led a team of RTL engineers to implement an EDGE WWAN solution in tandem with teams in two other locations. Led system engineering engagement with customers for EDGE WWAN solution.

Senior Member of Technical Staff
1996 - 2000 (4 years)

Advanced Development Labs. Due diligence for ADSL technology license. System architect for ADSL solutions that were spun-out of AMD as part of Legerity. Various advanced PC and communication projects, including leading a multi-site team to define and develop new xDSL technology software prototypes. Significant involvement with chipset, processor, and PC system communication and networking roadmaps.

Senior Member of Technical Staff
April 1995 - 1996 (1 year)

Multimedia group. Definition and specification for a family of programmable media processors targeted primarily at PC communications and telephony. Selected partners for technology acquisition, and followed through by acquiring and leading staff to perform technology transfers and modification to align with rapid time to market goals.

LifeWorks
Volunteer
August 2004 - May 2008 (3 years 10 months)

I am a volunteer, serving meals once a week, to teens who are homeless in Austin and being served by LifeWorks (www.lifeworksweb.org).

Mission Committee, Covenant Presbyterian Church
Co-Chair of Evangelism Division
January 2005 - April 2008 (3 years 4 months)

Co-chair of the evangelism division within the mission committee of Covenant Presbyterian Church (www.covenant.org).

Interfaith Hospitality Netowrk (Foundation for the Homeless)
Volunteer
2004 - 2008 (4 years)

Overnight volunteer for Interfaith Hospitality Network in Austin, in associatin with Foundation for the Homeless. IHN hosts homeless families in Austin, providing a safe place to stay in a church while the family is supporting by transitional services to get them back on their feet.

Home Phone Network Alliance (HPNA)
Standards Chair
1998 - 2001 (3 years)

Responsible for all external liaisons from HPNA to external groups, including ITU SG15, and IEEE 802. Supported rapid ITU-T publication of G.pnt (G.989)

ITU-T SG15 (Q4/15)
Associate Rappoteur, Editor (G.lite.bis) (G.992.4)
1997 - 2001 (4 years)

Responsible for editing of the upper layer protocols for G.dmt.bis (G.992.3) and G.lite.bis (G.992.4). Responsible for running semi-monthly meeting sessions with more than 100 participants from all over the globe. Member. Major roles in the publication of G.lite (G.992.2), including editing the power management chapter. Participated in supporting groups including T1E1.4, TR30, UAWG, US Preparatory Study Group B that worked in tandem to bring the ADSL standards to international status rapidly.

Tensleep Design Inc.
VP of Advanced Technology and Development
1993 - 1995 (2 years)

Led and managed the engineering group of this fab-less semiconductor manufacturer. Worked to migrate the VLSI core designs to standard cell to expand existing licensing business, and ported the DSP software technology to other platforms to create new business opportunities. Worked within the executive team and with customers to develop models for new products and applications of the mixed-signal technology. Analyzed various technologies for application to datacom, consumer, video, and games.

Tensleep Design, Inc.
Chief Engineer
1987 - 1993 (6 years)

Architected solutions for a V.29 data pump mixed signal chip, using DSP assembly code in a proprietary DSP core with on-chip sigma delta analog. Improved this technology to include higher modem speeds and lower system costs by increasing cycle rate and architecture efficiency and by integrating

a general purpose MCU processor. Provided full manpower and equipment requirements, schedules, and budgets. Assembled, led, and managed a superior team to implement these products using custom design. Wrote and optimized DSP high level and assembly code routines.

AMD
Design Engineer
May 1984 - 1987 (3 years)

Modem & SLAC groups. Specification and design of a CMOS sub-system using CAD tools. Prototyped the unit in TTL and developed test vectors. System level debug and optimization of a 100K gate 1200bps modem using a full gate prototype. Test, CAD, and debug strategies developed to support this same chip. Provided vision and leadership for re-engineering of a money making but older project using modem CAD methods.

Education

The University of Texas at Austin
MSEE, Electrical Engineering · (1984 - 1987)

Texas A&M University
BS, EE · (1980 - 1984)

Borger High School
· (1976 - 1980)

Contact

www.linkedin.com/in/doug-duschatko-35bb67 (LinkedIn)
www.caltexefficientenergy.com (Personal)

Doug Duschatko

Independent Semiconductors Professional
Austin

Summary

Microprocessor design, x86, Computing system design, Telecommunication switching design, SONET, IP, Optical switching. Lighting Expert

Experience

Caltex Efficient Energy, LP
President
August 2006 - Present (15 years 7 months)

Creating awareness of global warming issues and providing products and consulting services to businesses and residences about how they can reduce their energy consumption.

Independent Consultant
July 2002 - Present (19 years 8 months)

Flow Engines
VP of Engineering
September 2001 - June 2002 (10 months)

Cisco Systems
Director of Engineering
June 1998 - April 2001 (2 years 11 months)

Design and implementation of optical telecommunication switching devices.

Cyrix Corporation
Director of Engineering
January 1991 - June 1998 (7 years 6 months)

Management of engineering teams involved in microprocessor design and production

Solbourne Computer
Director, IC Design
1987 - 1991 (4 years)

Motorola
Design Engineer
1980 - 1987 (7 years)

Education

The University of Texas at Austin
BSEE, Electrical Engineering, Computers · (1976 - 1980)

Contact

www.linkedin.com/in/georgephoekstra (LinkedIn)
www.freescale.com/ (Company)

Top Skills

Circuit Design
SoC
Semiconductors

Patents

Circuit and method for latch bypass

Memory system with error correction and method of operation

Processor controlled command port architecture for flash memory

Randomly accessible memory having time overlapping memory accesses

Asymmetrical digital subscriber line (ADSL) block encoder circuit and method of operation

George P. Hoekstra

IP Technical Consultant
Austin

Summary

I am an intellectual property technical expert with extensive experience mining patents and drafting claim charts related to memory design. I have experience with both reverse engineering and system level claim charting. I have worked on a number litigation matters in both the U.S. District Court and the International Trade Commission.

Related Experience:
• Mining patent assets in the area of memory design
• Patent claim charting for patent assertion
• Litigation support for U.S. District Court and International Trade Commission actions
• Review of claim construction for Markman hearing
• Patent sales customer reviews
• 25+ U.S. Patents including Freescale patent of the year

Skills:
• DRAM memory design
• SRAM memory design
• NVM memory design

Experience

George P. Hoekstra LLC
Technology Consultant
December 2014 - Present (7 years 3 months)
Austin, Texas

Intellectual property consultant. Patent mining and litigation support.

Freescale Semiconductor
25 years 10 months

IP Circuit Design Specialist
January 2007 - October 2014 (7 years 10 months)
Austin, Texas

Patent licensing support, including drafting claim charts.
Patent litigation preparation, including both claim charting and claim construction support.
Patent sales support with claim charts and review with customers.

Circuit Design Manager
April 2004 - January 2007 (2 years 10 months)
Austin, Texas

Helped launch e500 based networking PowerPC chip. Hiring manager and team lead for embedded processor core design.

Circuit Designer
January 1989 - April 2004 (15 years 4 months)
Austin, Texas

Design of level one Cache. Design of error correction system for ADSL chip set. Embedded register file and SRAM designs. Specialty DRAM system design.

Intel Corporation
NVM memory designer
August 1986 - January 1989 (2 years 6 months)
Folsom, California

Data path design of first embedded controller based Flash memory.

Education

University of Minnesota
BSEE, Electrical Engineering

Contact

www.linkedin.com/in/alfredo-linz-67b3a0b (LinkedIn)

Top Skills

Digital Signal Processors
Semiconductors
Analog

Languages

English
Spanish

Publications

A Low-Power PLA for a Signal Processor
Efficient Implementation of an I-Q GMSK Modulator

Patents

Frequency ratio estimation arrangement and method thereof
Monolithic PC audio circuit with enhanced digital wavetable audio synthesizer
Monolithic PC audio circuit
Digital-to-analog converter with no offset-induced errors
Arrangement for asynchronous decimation using a frequency ratio estimator and method thereof

Alfredo Linz

Systems Engineer/ Architect at Looking at Opportunities
Austin

Summary

System, integrated circuit architecture and algorithm development, analysis, design and simulation.

Experience

Looking at Opportunities
Systems Engineer/ Architect
2014 - Present (8 years)
Austin, Texas

System, integrated circuit architecture and algorithm development, analysis, design and simulation.

Cirrus Logic
Staff Power Systems Engineer, Energy, Exploration and Lighting Division (EXL)
July 2009 - 2014 (5 years)
Austin, TX

Application of DSP and digital control to power electronics, mainly in the areas of power factor correction, power supplies and LED lighting.

- Control optimization of PFC circuits for various load types (resistive, constant current, constant power). Replaced trial and error compensator design method with a Matlab tool based on thorough system analysis and modeling.
- Trained the applications group in the use of the tool; improved capability to support customers with different needs in a timely manner.
- Developed efficiency optimization method for a power supply based on switching frequency variation as a function of load. Patent filed.
- Architected system for LED color control for incandescent dimming in a 2-string light bulb as a function of dim level and temperature. Electrical, thermal and optical (color) modeling and development of a software tool for the customer in Matlab and Excel. Enabled the division to enter a new segment of the LED market. Patent filed.
- Algorithm to minimize on-chip power in dimmable systems; led 3 person team for simulation, verification and implementation. Patent filed.

• Matlab/Simulink test benches for automatic characterization of system-level designs, including source and load blocks specified by current standards. Improved test time and reusability across projects.
• Developed a Simulink library implementing the instruction set of a custom DSP used for power control ICs. Enabled designers to assess finite precision effects and estimate computational load.
• Statistical analysis of fundamental noise limitations in a voltage reference curvature compensation method based on curve fitting using tester data. Derived quantitative requirements for measured data quality to meet desired tempco.

• Other : fast link PFC controller based on ripple cancellation using adaptive filter, interleaved PFC controller, stand-alone software model for PMSM and BLDC electrical machines with application to field-oriented control (FOC).

Integral Wave Technologies
Sr. Systems Architect
April 2004 - January 2009 (4 years 10 months)

Architecture definition, analysis, modeling, block performance specification, control algorithm design and implementation for a variety of DC-DC power conversion circuits including switched-C stack converters, charge pumps, charge pump-LDO hybrids, switching buck converters

Celite Systems
Member of Technical Staff
April 2002 - October 2003 (1 year 7 months)

Development of a wireline broadcast DSL system. Complete Matlab/Simulink based physical layer analysis and modeling including transformers, twisted-pair loop characterization, signal and noise contributions, derivation of reach limits and requirements for A2D and D2A converters and filters. Integration of commercial AFE devices (Si3101 ADSL AFE, EESolutions ADC), design of decimation circuits, interpolated echo cancellers and adaptive algorithms for RFI suppression. Exploration of MIMO techniques to increase SNR.

Legerity Inc.
Engineering Fellow
August 2000 - March 2002 (1 year 8 months)

Development of a complete physical layer model for a DMT(OFDM) based ADSL MODEM using the Matlab/Simulink/Stateflow toolset. Based on AWARE technology and Legerity's line driver products (DSLDR,HVLDR)

for a combined voice-data system. Technical lead and main contributor of a 3 person team. Concurrent frequency- and time-domain modeling, where the frequency domain model is based on analysis of algorithm performance limits and the time-domain model is based on their actual DSP implementation. Estimation of achievable bit rates including effects of analog block noise, codec ADC/DAC quantization, echo cancelation limits, interference (ISI,ICI,external interferers), FFT leakage, equalization (FDQ and TEQ) performance and effects of linecard environment (transformers and balance networks) and voice signal images. Correlation of model predictions to lab measurements. Presentation of a series of seminars on the MODEM algorithms to the Systems Group and the FAE organization.

AMD
SMTS
1993 - 2000 (7 years)

1993-2000 :

• ISDN U- interface transceiver system design - algorithm development and simulation written in C.
• System design of a G.Lite ADSL transceiver for the central office. Derivation of requirements for analog front ends. Simulation of the system in SPW.

1993-1996:

• System level specification of decimation, interpolation and noise shaping architectures for the “Interwave” CD quality audio codec/synthesizer.
• Development of asynchronous sample rate conversion methods.

AMD
MTS
1988 - 1992 (4 years)

1991-1992

• Worked on the "SONIC" (PhOX) cordless phone chip. Patented two structures for GMSK modulation. Published paper in IEEE Transactions on Circuits and Systems.
• Defined, simulated and carried down to RTL level the architectures for hardware decimation and interpolation and noise shaping. Decimator was a bit serial implementation extending Candy’s structure from order 2 to order 3.
• Developed a recursive DTMF generation method based on difference equations.

• Assisted team with performance simulation of the whole CODEC+ADPCM path.
• Evaluated performance limits of the SONIC DSP architecture with a 16-bit performance objective. This involved fixed-point noise analysis and optimization of filter structures.

1988 -1990 –
• Worked on the 79C30 ISDN S-interface TE chip Main Audio Processor. Re-wrote microcode to meet performance objectives at small signal levels. Reduced the power consumption from 45mW to 2 mW, rearranging functions to reduce clock frequency and inventing a low-power interleaved PLA architecture. Published in IEEE JSSC Feb 1991.

Education

Southern Methodist University
MSEE,Ph.D., Electrical Engineering · (1979 - 1984)

Escuela Politécnica Nacional
Ingeniero en Electronica y Telecomunicaciones, Electrical Engineering · (1969 - 1974)

Contact

www.linkedin.com/in/xiaolin-lu-07919a2 (LinkedIn)

Top Skills

RTOS
Embedded Software
Embedded Systems

Xiaolin Lu

Fellow and Director of IoT Lab at Texas Instruments
Plano

Experience

Texas Instruments
R&D Manager

Texas Instruments, Dallas
R&D Manager
1996 - Present (26 years)

Taxas Instruments
R&D Manager
2002 - 2004 (2 years)

Microware Systems
Software Architect
1992 - 1996 (4 years)

Education

Indiana University Bloomington
· (1990 - 1992)

Property Search

Property ID: 439038 - Tax Year: 2022

General Information

Property ID	439038
Property Status	Active
Geographic ID	R-1202-002-0120-1
Property Type	Real
Property Address	1950 S Ballard Ave Wylie, TX 75098
Total Land Area	43,124 sq. ft.
Total Improvement Main Area	1,451 sq. ft.
Abstract/Subdivision	Colonial Acres Estates
Primary State Code	A (Residential Single-family)
Legal Description	COLONIAL ACRES ESTATES, BLK B, LOT 12

Owner Information

Owner ID	124908
Owner Name(s)	Mccoy William Dale
Exemptions	HS (General Homestead)
Percent Ownership	100.00%
Mailing Address	1950 S Ballard Ave Wylie, TX 75098-4812

2022 Value Information

Value information for Property ID 439038 in the 2022 tax year is unavailable. Value information for prior years may be available in the Value History section below.

Entities

Taxing Entity	Tax Rate	Collected By
GCN (Collin County)	0.168087 (2021 Rate)	Collin County Tax Office
JCN (Collin College)	0.081222 (2021 Rate)	Collin County Tax Office
SWY (Wylie ISD)	1.459800 (2021 Rate)	Collin County Tax Office

Improvements

Improvement #1	Residential
State Code	A (Residential Single-family)
Homesite	Yes
Market Value	
Total Main Area	1,451 sq. ft.

Detail #	Type	Year Built	Sq. Ft.
1	MA - Main Area	1973	1,451
2	AG - Attached Garage	1973	750
3	CP - Covered Porch/patio	1973	75
4	EP - Enclosed Porch	1973	255

Improvement #2	Residential
State Code	A (Residential Single-family)
Homesite	Yes
Market Value	
Total Main Area	n/a

Land Segments

Land Segment #1	Residential Single Family
State Code	A (Residential Single-family)
Homesite	Yes
Market Value	
Ag Use Value	n/a
Land Size	0.9900 acres 43,124 sq. ft.

Contact

www.linkedin.com/in/john-mchale-156b4a16 (LinkedIn)

Top Skills

Strategic Planning
Marketing
Marketing Strategy

John McHale

Entrepreneur, Board Member, CEO, Chairman, Information Security, Information Technology, Investor
Austin

Summary

Experienced Partner with a demonstrated history of working in the information technology and services industry. Strong entrepreneurship professional skilled in Public Speaking, Start-ups, Leadership, Marketing, and Strategic Planning.

Experience

Genesis inventions
Partner
April 2002 - Present (19 years 11 months)

BreakingPoint, Inc.
Chairman, Founder
January 2007 - August 2012 (5 years 8 months)
Austin, TX

Developed and manufactured cyber-attack test systems for equipment manufacturers and military.

TippingPoint Technologies
Chairman, CEO, Founder
June 2001 - February 2004 (2 years 9 months)
Austin, TX

Developed and manufactured first enterprise Intrusion Prevention Systems. NASDAQ:TPTI. Acquired by 3COM corporation 2004.

NetSpeed, Inc
Chairman, CEO, Founder
November 1996 - May 1998 (1 year 7 months)
Austin, TX

Developed and Manufactured high-speed DSL equipment for telcos. First DSL deployment in the world. Acquired by Cisco, System.

NetWorth, Inc

Chairman, CEO, Founder
April 1988 - April 1996 (8 years 1 month)
Dallas, TX

Designed and manufactured high-speed enterprise networking systems.

NASDAQ:NWTH. Acquired by Compaq, Inc. 1998.

Education

University of Dayton
BSEE · (1974 - 1978)

Contact

www.linkedin.com/in/celite (LinkedIn)
www.monoDrive.io (Company)

Top Skills

Mobile Applications
Product Marketing
Machine Learning

Patents

System and method for determining the transmit power of a communication device operating on digital subscriber lines

System and method for determining the data rate capacity of digital subscriber lines

System and method for determining a communication protocol of a communication device operating on digital subscriber lines

DATA MAPPING INTERFACE

System and method for determining the transmit power of a communication device operating on digital subscriber lines

Celite Milbrandt

NI Fellow at NI (National Instruments)
Austin

Summary

• 20 years of experience bringing new and innovative technology to automotive, social media, web applications, and mobile applications.
• Created leading Internet Radio Business using machine learning with over 30 million active listeners.
• Successful performance in high-energy, fast-paced start-ups—RideScout, Slacker, and Celite Systems—as well as in established environments— Daimler, Cisco Systems, and Texas Instruments.
• Inventor holding 7 patents.

Specialties: Artificial Intelligence Machine learning, iOS, Android, Google App Engine, C++, Python, Django, marketing, business development, technical leadership, product definition, and feature prioritization

Experience

NI (National Instruments)
NI Fellow
April 2021 - Present (11 months)
Austin, Texas, United States

Support NI's accelerated growth in ADAS/AD simulation and test.

monoDrive [acquired by NI]
Chief Executive Officer
May 2016 - April 2021 (5 years)
Austin, Texas Area

monoDrive is the leader in simulating realistic vehicle and pedestrian behavior for vehicle safety and autonomous mode feature testing. The monoDrive simulator is recognized by top AI researchers, automotive manufactures, insurance agencies, and vehicle sensor manufactures as the leading platform for realistic ADAS/AV simulation for Camera, Radar, LiDAR, and Ultrasonic for advanced perception, planning, and control testing.

RideScout [acquired by Daimler]
Chief Product Officer
November 2013 - April 2016 (2 years 6 months)

Design and build stuff.

Slacker [acquired by LiveXLive]
VP, Director, Founder
November 2003 - June 2008 (4 years 8 months)

Slacker is one of the largest online Internet Radio Providers (next to Pandora) in US and Canada with more than 30 million active listeners.
-Developed the original business plan including market sizing, marketing plan, product definition, engineering budget, and deployment schedule for Slacker's music services business.
-Presented the plan to various potential business partners and investors resulting in over $80M in venture capital equity investment.
-Authored and published patent-pending idea "Systems and devices for personalized rendering of digital media content" for personalization of music content based on user profile. This concept is also known as Selective Storing.

Front page Wall Street Journal article (June 18th, 2007)

http://online.wsj.com/article/SB118213164387538671.html

Celite Systems
CTO, Director, Founder
2001 - 2003 (2 years)
Austin, Texas

Celite Systems was a VC Funded Startup building High Speed Internet Protocol Access Equipment for US and International Telecommunications Providers.
-Developed the business plan including market sizing, marketing plan, product definition, engineering budget, and deployment schedule for the Celite Systems product line.
- Presented the plan to various potential business partners and investors resulting in over $30M in venture capital equity investment.
- Invention of point to multipoint DSL utilizing single carrier 256 quadrature amplitude modulation (QAM) in the downstream and 16 quadrature amplitude modulation (QAM) time domain multiple Access (TDMA) for upstream.

Cisco Systems

Marketing
1997 - 2001 (4 years)

Cisco Systems Access Business manufactured and development voice band and broadband equipment for the largest telecommunications customer in the world.

- Invention, patent publishing, and productization of several novel adaptive learning techniques applied to spectral management, bandwidth optimization, and communication reliability improvement.
- Facilitated technical presentations with industry experts/analysts, standards bodies, partners, and customers.
- Assisted business development team providing technical due diligence on acquisitions and strategic investments.
- Acted as Cisco System's representative at the International Telecommunications Union (ITU) and the American National Standards Institute (ANSI) petitioning to include various technical strategies that aligned with Cisco Systems technology deployment strategy.

Amati Communications Corporation
dsp engineer
1997 - 1998 (1 year)

Education

California Polytechnic State University-San Luis Obispo
Engineering, Electrical Engineering · (1992 - 1996)

Contact

www.linkedin.com/in/vijayakumaran-nair-72292 (LinkedIn)

Top Skills

EDA
Digital Signal Processors
Mixed Signal

Vijayakumaran Nair

Principal Engineer at Intel Corp (Retired)
Austin

Summary

Specialties: IC design management
Sigma delta based data converters
Mixed signal circuits & systems design
Fuel Gauging for battery management
Integrated Digital Thermal Sensors
DSP algorithms and hardware
UWB

Experience

Intel Corporation
Principal Engineer (Retired)
January 2000 - June 2014 (14 years 6 months)

Advanced Micro Devices
Design Engineering Manager
August 1984 - December 1999 (15 years 5 months)

Mitel Corporation
Applications Engineering Manager
August 1982 - August 1984 (2 years 1 month)

1982 to 1983: Senior Hardware Engineer in Mitel Corporation

1983 to 1984 Applications Engineering Manager in Mitel Semiconductor

Central Dynamics Ltd
Senior Engineer
1980 - 1982 (2 years)

Indian Space Research Center
Engineer
1973 - 1979 (6 years)

Education

Carleton University

M.Eng, Electronics (1983) · (1979 - 1983)

College of Engineering Trivandrum

B.Sc (Engg), Electronics&Communications · (1968 - 1972)

Contact

www.linkedin.com/in/matt-pendleton-b68a204 (LinkedIn)

Top Skills

FPGA
DSP
Ethernet

Matt Pendleton

Principal at Ribbon Communications
Cedar Park

Experience

Ribbon Communications
Principal
October 2017 - Present (4 years 5 months)
Austin, Texas Area

Genband
Principal Engineer
March 2010 - Present (12 years)
Austin, Texas

various enterprises
Electronics Design Consultant
2007 - 2010 (3 years)

Genband
Principal Engineer
1999 - 2008 (9 years)

Motorola, Inc.
Senior Member Technical Staff
1987 - 1999 (12 years)

Texas Instruments
Design Engineer
1982 - 1987 (5 years)

Education

The University of Texas at Austin
MSEE, Engineering · (1985 - 1992)

University of Cincinnati
BSECE, Engineering · (1977 - 1982)

US005608643A

United States Patent [19]

Wichter et al.

[11] **Patent Number: 5,608,643**

[45] **Date of Patent: Mar. 4, 1997**

[54] **SYSTEM FOR MANAGING MULTIPLE DISPENSING UNITS AND METHOD OF OPERATION**

[75] Inventors: **Martin A. Wichter**, Arlington; **Tom R. Pohrte**; **Jack A. Ross**, both of The Colony; **Ray G. Sadler**, Plano, all of Tex.

[73] Assignee: **General Programming Holdings, Inc.**, Dallas, Tex.

[21] Appl. No.: **300,483**

[22] Filed: **Sep. 1, 1994**

[51] **Int. Cl.**[6] **G06F 17/00**

[52] **U.S. Cl.** **364/479.14**; 364/479.11; 364/479.12; 221/9

[58] **Field of Search** 364/478, 478.01–479.14; 194/217; 221/9; 340/825.35

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,241,237	12/1980	Paraskevakos et al. .	
4,412,292	10/1983	Sedam et al.	364/479
4,766,548	8/1988	Cedrone et al.	364/479
4,999,763	3/1991	Ousborne	364/478
5,029,098	7/1991	Levasseur	364/479
5,091,713	2/1992	Horne et al.	364/479
5,282,127	1/1994	Mii	364/479

OTHER PUBLICATIONS

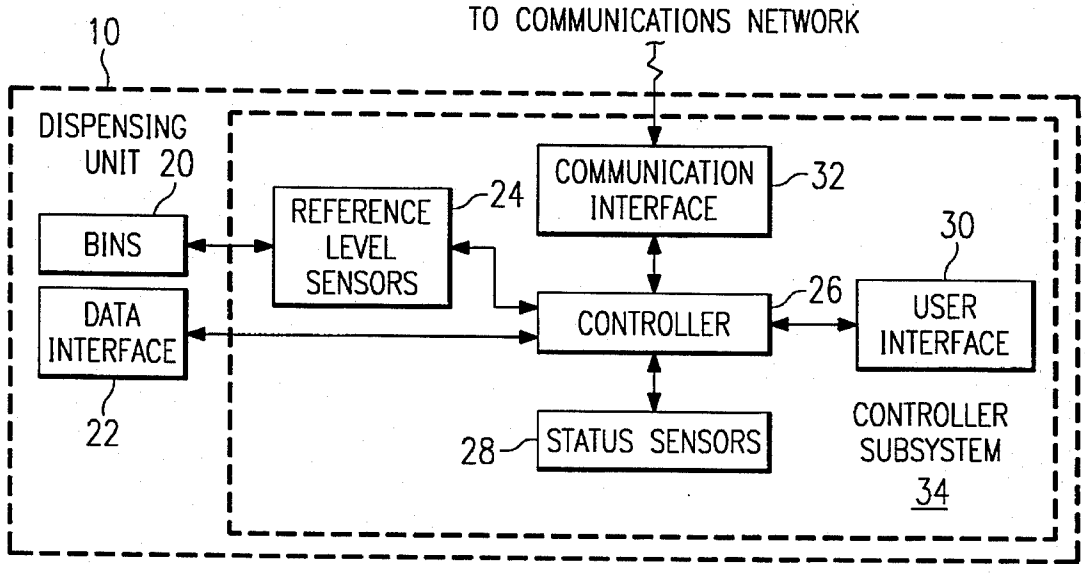
Wichter, Martin A., Declaration of, including Exhibit; brochure, "*Vending–Manager*™", copyright 1992.

Primary Examiner—Roy N. Envall, Jr.
Assistant Examiner—Steven R. Garland
Attorney, Agent, or Firm—Baker & Botts, L.L.P.

[57] **ABSTRACT**

A system (**8**) for managing multiple dispensing units by communicating information through a communications network (**12**) is provided. The system includes a plurality of dispensing units (**10**) operable to transmit and receive information through the network. Each dispensing unit includes a plurality of bins (**20**) operable to hold a quantity of product. Each dispensing unit includes a plurality of reference level sensors (**72**) where each reference level sensor is coupled to an associated bin. Each reference level sensor is operable to determine when the quantity of product in the associated bin drops below a reference level (**76**) that is higher than an out of stock level (**82**) of the associated bin. Each dispensing unit includes a controller subsystem (**34**) coupled to the plurality of bins, to the plurality of reference level sensors, and to the network. The controller subsystem is operable to monitor conditions of the dispensing unit, to transmit status messages responsive to an occurrence of one of a plurality of defined events, and to receive command messages. The system further includes a dispensing unit controller system (**14**) operable to communicate through the network. The dispensing unit controller system is operable to receive status messages from each of the dispensing units, to process the status messages, and to transmit command messages to each of the dispensing units. One command message can be an instruction to a dispensing unit to download a software module to update an existing software module in the controller subsystem of the dispensing unit.

24 Claims, 9 Drawing Sheets



US005392299A

United States Patent [19]

Rhines et al.

[11] **Patent Number: 5,392,299**

[45] **Date of Patent: Feb. 21, 1995**

[54] **TRIPLE ORTHOGONALLY INTERLEAED ERROR CORRECTION SYSTEM**

[75] Inventors: **Don S. Rhines**, Richardson; **William D. McCoy**, Wylie, both of Tex.; **Kirk H. Handley**, Redwood City, Calif.

[73] Assignees: **E-Systems, Inc.**, Dallas, Tex.; **Ampex Corporation**, Redwood City, Calif.

[21] Appl. No.: **820,737**

[22] Filed: **Jan. 15, 1992**

[51] **Int. Cl.**[6] **G06F 11/10**

[52] **U.S. Cl.** **371/37.5**; 371/37.4

[58] **Field of Search** 371/37.4, 37.5, 37.7

[56] **References Cited**

U.S. PATENT DOCUMENTS

Re. 30,187	1/1980	Hong et al.	371/37.4
Re. 31,311	7/1983	Miller	360/40
3,786,439	1/1974	McDonald et al.	371/37.4
3,868,632	2/1975	Hong et al.	371/37.4
4,413,340	11/1983	Odaka et al.	371/38.1
4,541,091	9/1985	Nishida et al.	371/37.5
4,567,594	1/1986	Deodhar	371/38.1
4,598,403	7/1986	Odaka	371/39.1
4,637,021	1/1987	Shenton	371/37.5
4,677,622	6/1987	Okamoto et al.	371/37.5
4,680,764	6/1987	Suzuki et al.	371/37.5
4,730,321	3/1988	Machado	371/38.1
4,742,517	5/1988	Takagi et al.	371/37.4
4,802,170	1/1989	Trottier	371/40.1
4,852,099	7/1989	Ozaki	371/37.5
4,852,102	7/1989	Yamaguchi	371/37.4

FOREIGN PATENT DOCUMENTS

0273676A2	12/1987	European Pat. Off. .
0341851A3	4/1989	European Pat. Off. .
0551973	7/1993	European Pat. Off. .
55-35562	3/1980	Japan .

OTHER PUBLICATIONS

"Concentrated Coding Systems Employing a Unit–Memory Convolution Code and a Byte-Oriented Decoding Algorithm", Lin–Nan Lee, IEEE transactions on Communications, vol. COM–25, No. 10, Oct. 1977, pp. 1064–1074.

"Reliability and Throughput Analysis of a Concatenated Coding Scheme," R. H. Deng, *IEEE Transactions on Communications,* vol. COM–35, No. 7, Jul., 1987, pp. 698–705.

"The Design of High Performance Error–Correcting Coding Scheme for the Canadian Broadcast Telidon System Based on Reed–Solomon Codes," B. C. Mortimer, et al., *IEEE Transactions on Communications,* vol. COM–35, No. 11, Nov., 1987, pp. 1113–1122.

"Error Control Codes for Digital Recording Systems," S. W. Kim, *IEEE Transactions on Consumer Electronics,* Nov., 1989, pp. 907–916.

"Reed–Solomon Error and Eraser Corrections for PAM/FM Mobile Radio Systems," G. D. Aria, *IEEE 38th Vehicular Technology Conference,* 1988, pp. 485–488. (Month Unknown).

"A New Two–Inch Data Disc System with a High Transfer Rate," K. Kutaragi, et al., *IEEE Transactions on Consumer Electronics,* vol.–C–33, No. 4, Nov., 1987, pp. 540–550.

"Performance of Simple Cross–Interleaved Reed–Solomon Decoding Strategies for Compact Disc Players," C. C. Ko, et al.,—*International Journal of Electronics,* 1988, vol. 64, No. 4, pp. 627–635.

"Error Correction, Interleaving and Differential Pulse Position Modulation," R. E. Peile, *International Journal of Satellite Communications,* vol. 6, Jan. 1988, pp. 173–187.

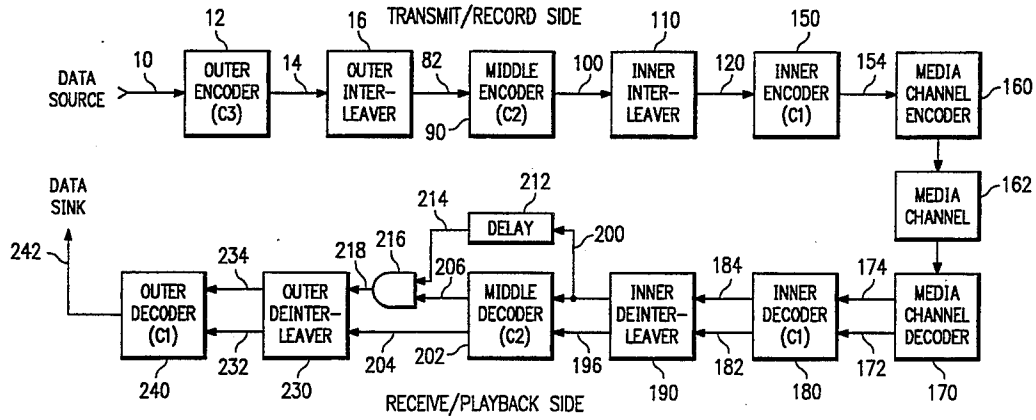
Primary Examiner—Paul Gordon

Attorney, Agent, or Firm—Harold E. Meier

[57] **ABSTRACT**

The detection and correction of errors in digital data transmitted by or stored in a media channel is provided by processing the data through a triple orthogonally interleaved error correction system. On the transmit/-store side of the system, the data is encoded three times prior to placement in the media channel with two different interleaving steps performed between the encoding steps. The first interleave is an orthogonal row shuffling interleave that provides enhanced protection against burst errors. On the receive/play back side, the data is decoded and deinterleaved, with included errors detected and corrected to enable recovery of the original data. To enhance the error correction, a circuit is used for generating a symbol accurate error flag identifying symbols containing errors thereby allowing the error correcting decoders to focus on and correct the data.

63 Claims, 14 Drawing Sheets



Contact

www.linkedin.com/in/mat-rybicki-6aa45b10 (LinkedIn)

Top Skills

Semiconductors
Mixed Signal
Analog

Mat Rybicki

President & CEO at Forge Tech, Inc.
Austin

Experience

Forge Tech, Inc.
11 years 6 months

President & CEO
January 2015 - Present (7 years 2 months)
Kemah, TX

Forge Tech, Inc. is an engineering and technology company with a patented metal bonding technology. Currently, Forge Tech, Inc. is providing services to the Petrochemical and Energy Industries and licensing their technology to service providers.

Member, Board of Directors
September 2010 - Present (11 years 6 months)
Kemah, TX

Forge Tech, Inc. is an engineering and technology company with a patented metal bonding technology. Currently, Forge Tech, Inc. is providing services to the Petrochemical and Energy Industries and licensing their technology to service providers.

ERCT
President of the Board
June 2015 - Present (6 years 9 months)
Leander, Texas

Serving as President of the Board of Equine Rehabilitation Central Texas (ERCT), a non-profit organization that provides equine assisted therapy to Veterans with PTSD and to individuals with developmental disabilities.

Austin International Rescue Operations, Inc. (AIRO)
Member, Board of Directors
April 2005 - Present (16 years 11 months)

Tardust, LLC
Executive Producer
March 2012 - March 2019 (7 years 1 month)
Austin, TX

Involved in the production of the independent film, "Angels In Stardust".

Mathew Rybicki, Consulting
Consultant
2006 - January 2015 (9 years)

Inventor, investor and entrepreneur.

Austin International Rescue Operation, Inc. (AIRO)
COO
January 2010 - December 2012 (3 years)

Disaster rescue, relief and reconstruction, focused on Indonesia and Haiti

ViXS Systems Inc.
8 years 9 months

Member, Technical Advisory Board
January 2006 - December 2009 (4 years)

VP Engineering
April 2001 - December 2005 (4 years 9 months)

SigmaTel
VP Engineering
September 1996 - December 2000 (4 years 4 months)

Motorola Semiconductor
Engineer and Manager
1983 - 1996 (13 years)

Education

Texas A&M University
MS Electrical Engineering, Engineering · (1981 - 1983)

Texas A&M University
BS Electrical Engineering, Engineering · (1976 - 1981)

Contact

www.linkedin.com/in/donald-shaver-a131626 (LinkedIn)
extennovationip.com (Company)
www.comtorics.com (Company)

Donald Shaver

Sensco Solutions Inc. Chief Architect
Dallas

Summary

Chief Architect at Sensco Solutions, Consultant at Comtorics Information Systems and Consulting® LLC and ExtennovationIP

Specialties: embedded systems hardware and software, signal processing, semiconductors, wireless and wireline communications, networking, optimization algorithms, standards development

Experience

Comtorics Information Systems and Consulting® LLC
Founder
February 2014 - Present (8 years 1 month)

Don is President and Founder of Comtorics Information Systems and Consulting® LLC. The focus of Comtorics is developing systems, algorithm, and software technology. Don has been a technical leader in industry for many years. He has developed complete systems, software, and hardware driven solutions starting in the Defense and Seismic Services industries. While in the semiconductor industry, he established and led several R&D initiatives, and standards development in video compression (ISO/IEC MPEG2) , multimedia signal processing, and communications solutions (DSL, HomePNA™, IEEE 802, Wi-Fi®, WiMAX™, 3G / 4G-LTE, and IEEE 1901.2 PLC). Don has worked in standards development organizations including IEEE, ITU, ISO/IEC, and SAE. Don is inventor on 18 U.S. issued patents. Don earned a PhD and Master's degree from Syracuse University in Systems and Information Science. He also earned a BS degree in Electrical Engineering from Syracuse. Don is an active member of SAE, ASME, SEG, and IEEE (Computer, Communications, Circuits, and Power Societies).

ExtennovationIP
Consultant
May 2015 - Present (6 years 10 months)

Don is an independent consultant with Extennovation Intellectual Properties. ExtennovationIP provides a unique IP Asset harvesting and IP creation service

focused on developing and accelerating intangible assets. ExtennovationIP operates globally, with headquarters in France. During development of a new product, ExtennovationIP recommends that regular IP Harvesting and IP Creation be conducted to ensure that the intellectual property generated by a company's R&D teams is identified, categorized, and appropriately protected. Supporting a cross functional team of engineers, marketing personnel and managers to explore ideas, ExtennovationIP can effectively develop innovations that are important for the future of the company. The resulting IP assets can be documented in a timely manner and filed with the clients' patent agencies or if appropriate protected as a formal trade secret. Don has R&D experience in mobile communications, semiconductors, smart grid, and multimedia systems, all with a focus on hardware, software, algorithms, and standardization.

Sensco Solutions
Chief Architect
2016 - Present (6 years)

Archimedes Intellectual Properties Ltd
Consultant
June 2014 - April 2015 (11 months)

Archimedes Intellectual Properties, Limited is made up of a team of award winning experts in business, law and engineering that can help to maximise the value of IP assets in any company worldwide. Our team features multiple members of the IAM300 list of leading IP Strategists globally. We offer bespoke solutions to clients in most industry sectors. Our services include, but are not limited to, Corporate IP Strategy Services, Virtual CIPO Services, IP Due Diligence Services, IP Audit & Corporate Governance Services, IP Budgeting Services, IP Asset Development Services, IP Asset Development Services, IP Business Advisory Services and White Label Services. At Archimedes, we focus on providing clients with practical advice that serves to enhance corporate revenue and net worth. Archimedes Intellectual Properties, Limited operates globally, with headquarters in the United Kingdom and the United States. (See www.archimedesip.com)

Texas Instruments
36 years 10 months

Chief Architect Smart Grid, Texas Instruments Fellow
July 2011 - October 2013 (2 years 4 months)
Dallas, Texas

Don Shaver is a Texas Instruments (TI) fellow and chief architect for TI's Smart Grid business unit, where he is responsible for systems-level concepts and defining new products. Don represents TI's Smart Grid solutions across industry standards organizations such as IEEE, ITU, PRIME, G3, and NIST, and drives TI's influence on governmental standards and regulatory activities. During his 20+-year career with TI, Don has held various positions in both product-specific and research and development organizations. He has initiated and directed new technology businesses, international standards development in wireless and wire line communications and he has developed systems, software, and application-specific processors in defense, geophysical, and communications applications. He has been awarded 15 patents. Don is vice-chair of the IEEE Computer Society Dallas Chapter and senior member of the IEEE. Don is also a member of ASME, SAE, and SEG. He earned a Bachelor of Science in electrical engineering as well as a Master of Science and Doctorate in systems and information science, all from Syracuse University.

Director, TI Fellow
August 1995 - August 2011 (16 years 1 month)

Director, Communications and Medical Systems Laboratory

Signal Processing Systems Center

12500 TI Boulevard

Dallas, Texas 75243

Director Digital Audio and Video Laboratory, Tsukuba, Japan
June 1990 - July 1995 (5 years 2 months)

Research Manager, DSP Applications
February 1987 - June 1990 (3 years 5 months)

Systems Engineering Manager, Land-Based Seismic Acquisition Systems
January 1980 - February 1987 (7 years 2 months)

Developed leading edge seismic acquisition systems for Geophysical Services Incorporated, a subsidiary of Texas Instruments

Systems Engineer, Advanced Narrowband Digital Voice Processor
January 1977 - January 1980 (3 years 1 month)

Education

Syracuse University

BSEE, MS, PhD, Electrical Engineering, Systems and Information Science

US006366644B1

(12) **United States Patent**
Sisk et al.

(10) **Patent No.: US 6,366,644 B1**
(45) **Date of Patent: Apr. 2, 2002**

(54) **LOOP INTEGRITY TEST DEVICE AND METHOD FOR DIGITAL SUBSCRIBER LINE (XDSL) COMMUNICATION**

(75) Inventors: **James R. Sisk**, Cedar Park; **John F. McHale**, Austin, both of TX (US)

(73) Assignee: **Cisco Technology, Inc.**, San Jose, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **08/929,778**

(22) Filed: **Sep. 15, 1997**

(51) **Int. Cl.**[7] **H04M 1/24**
(52) **U.S. Cl.** **379/1.04**; 379/27.01; 379/27.03; 379/1.01; 379/29.01
(58) **Field of Search** 379/5, 26, 27, 379/28, 29, 22–24, 18, 12, 10, 9, 6, 1, 1.01, 1.04, 22.02, 22.03, 22.04, 27.01, 27.03, 30; 370/247, 248, 249

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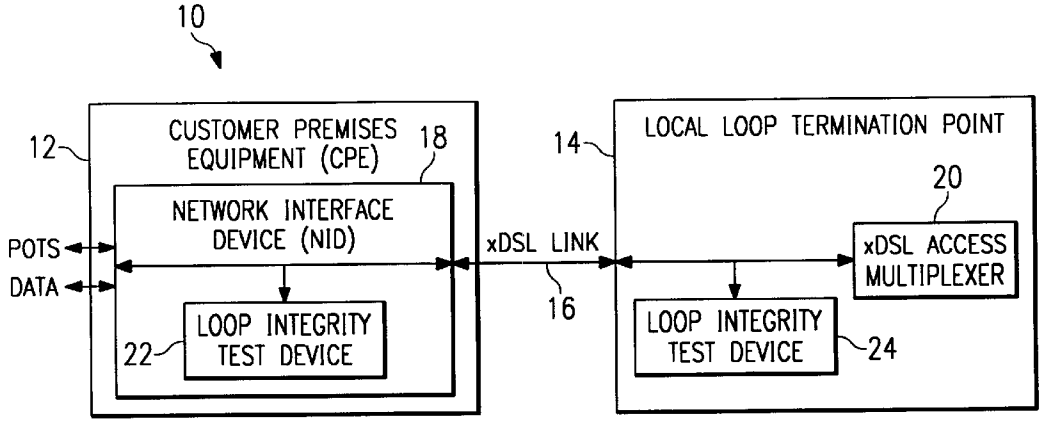
Horst Hessenmüller, et al., Zugangsnetzstrukturen für interaktive Videodienste (Teil 2), *Fernmelde–Ingenieur*, vol. 48, No. 9, XP000619688, Sep., 1994, Germany, pp. 1–28 (with English translation).

Primary Examiner—Curtis Kuntz
Assistant Examiner—Rexford N Barnie
(74) *Attorney, Agent, or Firm*—Baker Botts L.L.P.

(57) **ABSTRACT**

A digital subscriber line (xDSL) communication system **(10)** is disclosed that allows xDSL communication across a local loop. The system **(10)** includes a local loop termination point **(14)** and customer premises equipment **(12)** connected to a twisted pair telephone line **(16)**. Loop integrity test devices **(22, 24)** for xDSL communication are located at the local loop termination point **(14)** and the customer premises equipment **(12)** and are coupled to the telephone line **(16)**. The loop integrity test devices **(22, 24)** are respectively operable to transmit test signatures across the telephone line **(16)**, to receive and evaluate test signatures from the telephone line **(16)**, and to indicate whether the telephone line **(16)** can support xDSL communication based upon evaluation of test signatures.

12 Claims, 1 Drawing Sheet



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www.linkedin.com/in/andy-thurston-6145901 (LinkedIn)
www.yourgaragepros.com (Company)

Top Skills

Managed Services
Information Technology
Unified Communications

Andy Thurston

Owner of Dream Garage Specialists
Liberty Hill

Experience

Dream Garage Specialists
Owner
August 2013 - Present (8 years 7 months)
Liberty Hill, TX

In August of 2013, I purchased a very special company - Dream Garage Specialists. DGS specializes in custom cabinets and epoxy floors for garages. We are a privately held, family owned, local company that has been serving the Austin area for over 14 years. Our cabinets are custom built using a computerized CNC router. This gives us the capability to custom build cabinets to exact specifications for your garage. We have a local factory in Liberty Hill Texas, serving the greater Austin area.

Dream Garage was one of the first to offer epoxy floors in the Austin area back in 1999. We create an exceptional "Granite" looking floor utilizing a layer of paint chip embedded into the epoxy. Although paint chips are not uncommon, our process is unique. Standard paint chips mixes are available but we blend chips at our factory. Our mixing process creates a natural look with a variable size blend of chips.

We also offer Activity Organizer solutions by Organized Living. This is a grid based system that replaces the traditional slat wall. The grids are more durable than slat wall and still provide the same organizational flexibility.

TUC Managed IT Solutions
Owner
April 2012 - March 2013 (1 year)

TUC Managed IT Solutions is a leading provider of virtual IT service and support for small and medium-sized businesses delivering the required hardware, software and service for a monthly fixed fee per user. Our Connected Office® service program provides a single point of contact to deliver and manage technology, communications and vertical line of business applications – 95% Remote; 100% Proactive.

Cisco Systems

Senior Management - ASIC Design
September 1999 - July 2011 (11 years 11 months)

Manage teams architecting, developing, and implementing custom switching ASICs.

• Architecture tradeoffs, methodology and tools.
• Develop and present execution strategy to senior management: architecture/ feature content, project plans, budgets, risk assessment.
• Cross-functional interface with marketing, hardware, software, system test, and manufacturing.
• Vendor RFQ/selection, vendor engagement management and execution management.

Monterey Networks
ASIC Design
January 1999 - September 1999 (9 months)

Optical Cross Connect Company purchased by Cisco Systems at the height of the Telecom bubble (Sept '99).

Mentor Graphics
Design Consultant
June 1995 - December 1998 (3 years 7 months)

• Interface with customers providing diverse design services to Mentor’s major customers.
• Business development, contract development.
• ASIC/FPGA services – RTL, DV, methodology and tools.

STMicroelectronics
ASIC Design Engineer
February 1994 - June 1995 (1 year 5 months)
Carrollton, Texas

• ASIC physical design – place & route, DRC, Spice (.8u Gate Array).
• Second sourced disc drive controller ASIC for Seagate.
• Successful development resulted in $20M annual savings for the customer.

Raytheon
Senior Design Engineer
February 1984 - November 1993 (9 years 10 months)
Marlboro, Massachusettes

System Lead for 11 person team developing a custom Array processor (Raytheon Vector Processor) for satellite defense application.

• Lead architect – developed RISC based execution engines – instruction set development, unique multiprocessor synchronization mechanism.
• Developed system specification and architecture.
• Four PCB system utilizing ASIC and FPGAs.
• Various ASIC designs, board design, micro-code development, real time software development in C.

Education

Worcester Polytechnic Institute

MSEE, Electrical Engineering - Computer · (1985 - 1990)

Purdue University

BSEE, Electrical Engineering - Computer · (1980 - 1983)

US005751741A

United States Patent [19]

Voith et al.

[11] Patent Number: 5,751,741

[45] Date of Patent: May 12, 1998

[54] **RATE-ADAPTED COMMUNICATION SYSTEM AND METHOD FOR EFFICIENT BUFFER UTILIZATION THEREOF**

[75] Inventors: **Raymond Paul Voith; Sujit Sudhaman; George Hoekstra**, all of Austin, Tex.

[73] Assignee: **Motorola, Inc.**, Schaumburg, Ill.

[21] Appl. No.: **754,768**

[22] Filed: **Nov. 20, 1996**

[51] **Int. Cl.**[6] **H03M 13/22**

[52] **U.S. Cl.** **371/37.7**; 370/914; 371/2.2; 371/37.02

[58] **Field of Search** 371/37.02, 2.2, 371/37.7; 370/914

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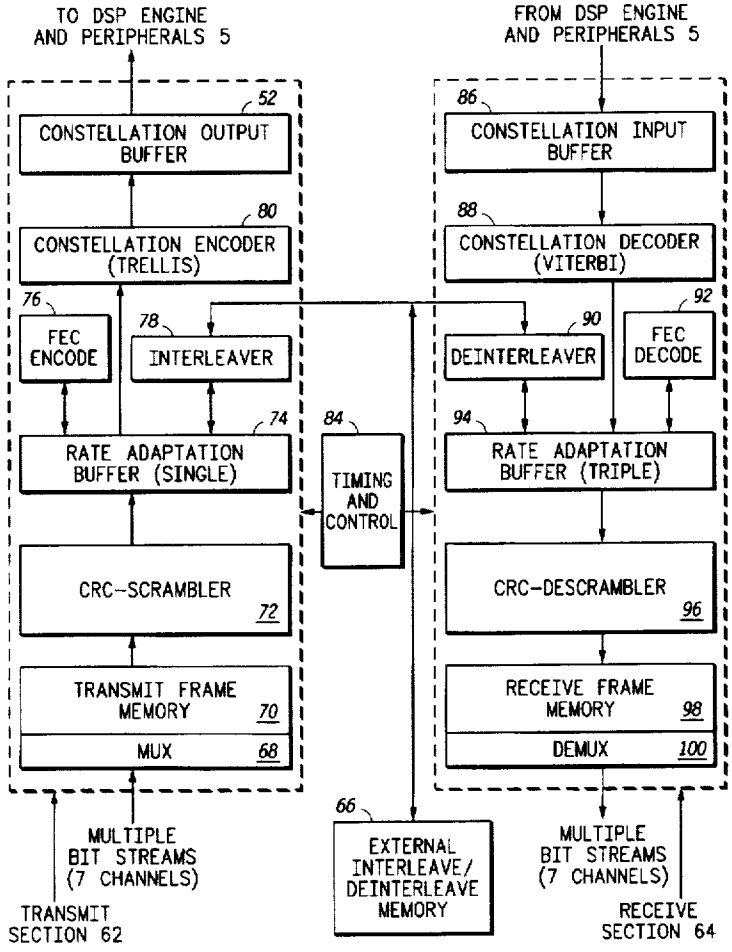
Primary Examiner—Stephen M. Baker

Attorney, Agent, or Firm—Daniel D. Hill; Paul J. Polansky

[57] **ABSTRACT**

A transceiver (**34**) includes a rate adaptation buffer (**74**) that synchronizes a data stream received at a 4.0 kHz rate to a data stream that is transmitted at a 4.05 kHz rate. A transmit section (**62**) of the transceiver (**34**) performs rate adaptation using a single rate adaptation buffer. The transmit section (**62**) includes four autonomous modules which are able to access the data in the rate adaptation buffer (**74**) independently of one another. These four modules include a CRC-scrambler (**72**), a FEC encoder (**76**), an interleaver (**78**), and a constellation encoder (**80**). A timing controller (**84**) prevents contention for accesses to the rate adaptation buffer (**74**). In addition, each of the four modules perform their respective functions quickly enough to prevent overflow or underflow conditions in the rate adaptation buffer (**74**). A receive section (**64**) functions similarly to the transmit section (**62**).

18 Claims, 6 Drawing Sheets



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Information Technology and Services Professional

Arlington

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Song Wu

Senior Staff Engineer at Xilinx
Plano

Experience

Xilinx
Senior Staff Engineer